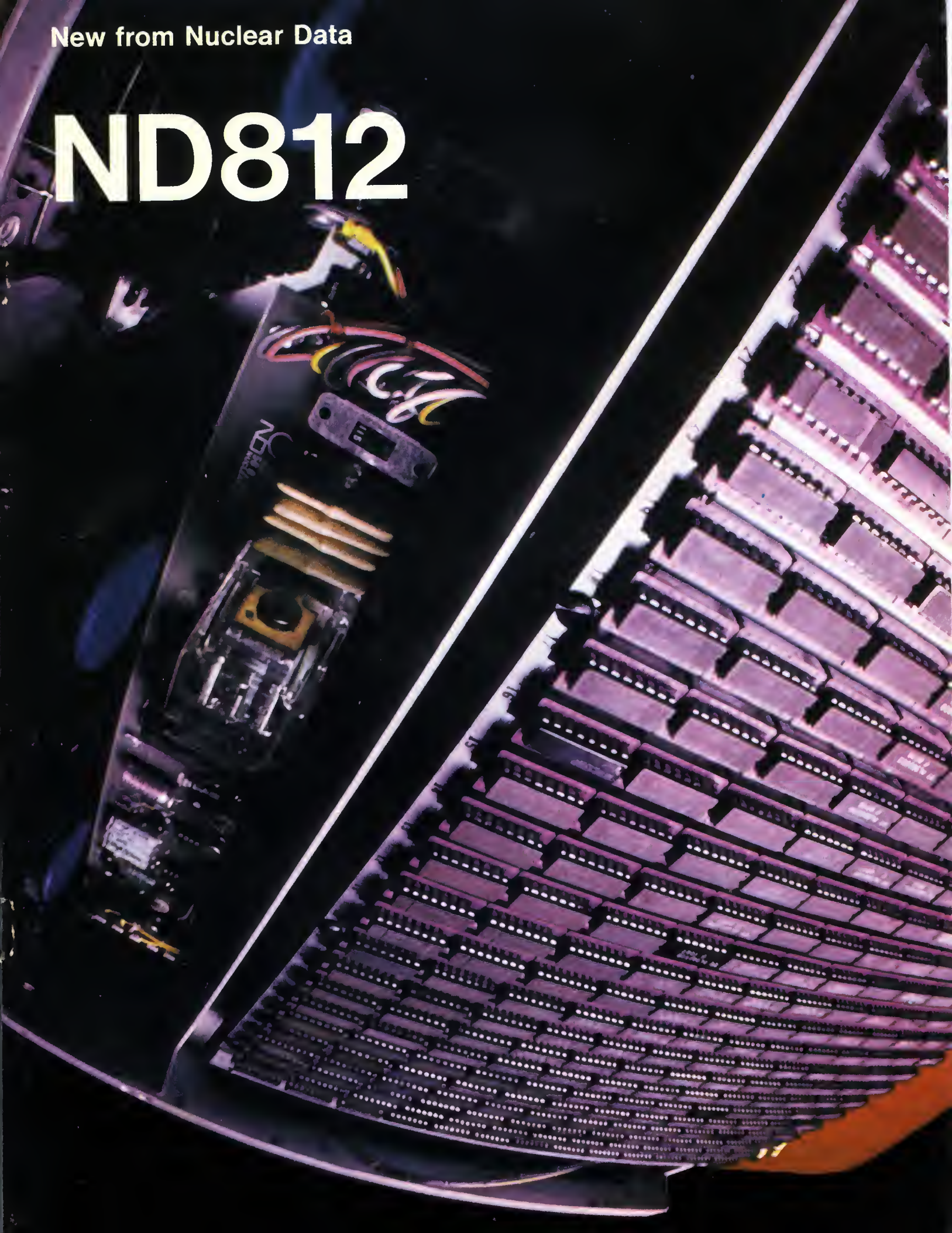
New from Nuclear Data

ND812



More core and
instruction capability...
dollar for dollar...
than any other computer
on the market

WHY A MINI-COMPUTER FROM NUCLEAR DATA?

Nuclear Data, Inc., started making special purpose computers in 1959. As experimental requirements grew in complexity we delivered complete systems which included a purchased general purpose computer. The systems are used for advanced experiments in various scientific fields.

In accepting total system responsibility the company developed a strong capability in all phases of computer system design—hardware, software, and peripheral interfaces.

With a computer at the heart of our systems it was logical for us to build our own processor, and to design it to give the research experimentalist maximum programming power at minimum cost.

The Nuclear Data processor is described in this brochure. Its price, instruction power, programming ease and I/O capability are outstanding. When you compare its features, operating advantages, and power with other computers in the same price range, we think you will agree it "stands alone."

ABOUT THE ND812

The ND812 is an 8K computer selling for less than $10,000. It is 12-bit machine, and we are asked why 12 and not 16 bits?

The answer is because we have been able to design a processor with the instruction power and programming ease of a 16-bit machine but at a much lower price.

Compare the following advantages of the ND812 with any 16-bit or 12-bit computer currently available.

Compare the Price:

The ND812 gives you 8192 words of core memory for less than $10,000. A quantity discount schedule applies to multiple unit orders.

Compare Instruction and Arithmetic Power:

Shown on pages 3 through 10, the ND812 instruction set speaks for itself. Note the 16 memory reference instructions, three literals, and the large number of arithmetic and register control instructions. The ND812 has double accumulators with individual sub-accumulators, and hardware multiply and divide are standard features.

Compare Addressing Capability:

The ND812 does not have traditional 12-bit processor addressing limitations. In addition to relative and indirect addressing, the entire 8192 words of core may be directly addressed using two-word instructions. The ND812 is also available in 4K and 16K memory configurations, field expandable. In the 16K configuration the entire 16,384 words of core may be directly addressed.

The two-word instruction, equivalent to a 21-bit instruction, is very convenient to use, particularly for the inexperienced programmer. In the ND812 the combination of two-word instructions and hardware multiple field control provides easy transit across 4K field boundaries, thus avoiding a problem common to other 12-bit processors.

Compare Input/Output Capability:

4-Level Priority Interrupt

This is a standard feature in the ND812. Level selection is programmable, and for each level, priorities are determined by the sequence in which devices are connected.

A peripheral device may trap to any specified core location in the first 4K of memory, thus eliminating polling requirements in the program. If no location is specified, it will automatically trap to location #1 in memory.

12 or 24-Bit Programmed I/O Transfer

The ND812 has the following capability per single I/O instruction: Transmit 12 or 24 bits; receive 12 or 24 bits; transmit 12 *and* receive 12 bits; receive 12 *and* transmit 12 bits. This capability is compatible with a 1, 2, or 3 byte oriented I/O structure.

Four Microprogrammable Pulses Per I/O Instruction

The last four bits of an I/O instruction may be used to provide voltage levels for device selection and they may also be used to generate four sequential pulses for peripheral control. These pulses make multi-function operation possible with a single I/O instruction.

4096 Possible I/O Commands

If the last four bits of the I/O instruction are used to provide voltage levels, a total of 256 I/O commands are possible with single word instructions at 3 μsec per instruction, and a total of 4096 I/O commands are possible with two-word instructions at 5 μsec per instruction.

Direct Memory Access (DMA)

In the ND812, DMA will operate at 6 megabits per second, and read, load, increment or *decrement* is possible on a single cycle.

For DMA operation the ND812 has a multiple precision line, controlled by peripheral device logic, which initiates automatic advances through successive core locations. Thus for a block transfer only the first address of the block need be specified.

For multiple precision arithmetic this feature is particularly useful. As an example, suppose on a DMA you want to increment a 24-bit number stored in two adjacent core locations. If an overflow occurs after the first location has been incremented, a carry signal from the processor to the peripheral results in an automatic advance and increment of the next core location. If the data word to be incremented occupies more than two locations, the automatic advance and incrementation may be repeated as many times as needed.

Compare Serviceability:

The ND812 central processor unit (CPU) consists entirely of integrated circuitry (97% MSI and TTL, 3% DTL) with no discrete components. The CPU's entire complement of IC's are mounted on a single wire-wrapped socket board, thus making every signal available and permitting simple replacement of IC's without soldering.

Users familiar with the problem of unsoldering and resoldering IC's on printed circuits boards will appreciate the advantages of this socket board.

A further advantage is a drastic reduction in the cost of spare parts. With the socket board, only IC's are needed, at considerably less cost than printed circuit boards or modules.

ND812 INSTRUCTION SET

Memory Reference Instructions:

SMJ	2400	Skip if lower accumulator (J) not equal to memory (TWSMJ 0240 is same instruction but as a two-word)
DSZ	3000	Decrement memory and skip if result is zero (TWDSZ 0300 is same instruction but as a two-word)
ISZ	3400	Increment memory and skip if result is zero (TWISZ 0340 is same instruction but as a two-word)
SBJ	4000	Subtract memory from lower accumulator (J) (TWSBJ 0400 is same instruction but as a two-word)
ADJ	4400	Add memory to lower accumulator (J) (TWADJ 0440 is same instruction but as a two-word)
LDJ	5000	Load lower accumulator (J) with memory (TWLDJ 0500 is same instruction but as a two-word)
STJ	5400	Store lower accumulator (J) in memory (TWSTJ 0540 is same instruction but as a two-word)
JMP	6000	Jump unconditionally (TWJMP 0600 is same instruction but as a two-word)
JPS	6400	Jump to subroutine (TWJPS 0640 is same instruction but as a two-word)
XCT	7000	Execute instruction at referenced address
ANDF	2000	Logical AND forward memory 12 bits with lower accumulator (J).
TWSMK	0250	Skip if upper accumulator (K) not equal to memory
TWSBK	0410	Subtract memory from upper accumulator (K)
TWADK	0450	Add memory to upper accumulator (K)
TWLDK	0510	Load upper accumulator (K) with memory
TWSTK	0550	Store upper accumulator (K) in memory

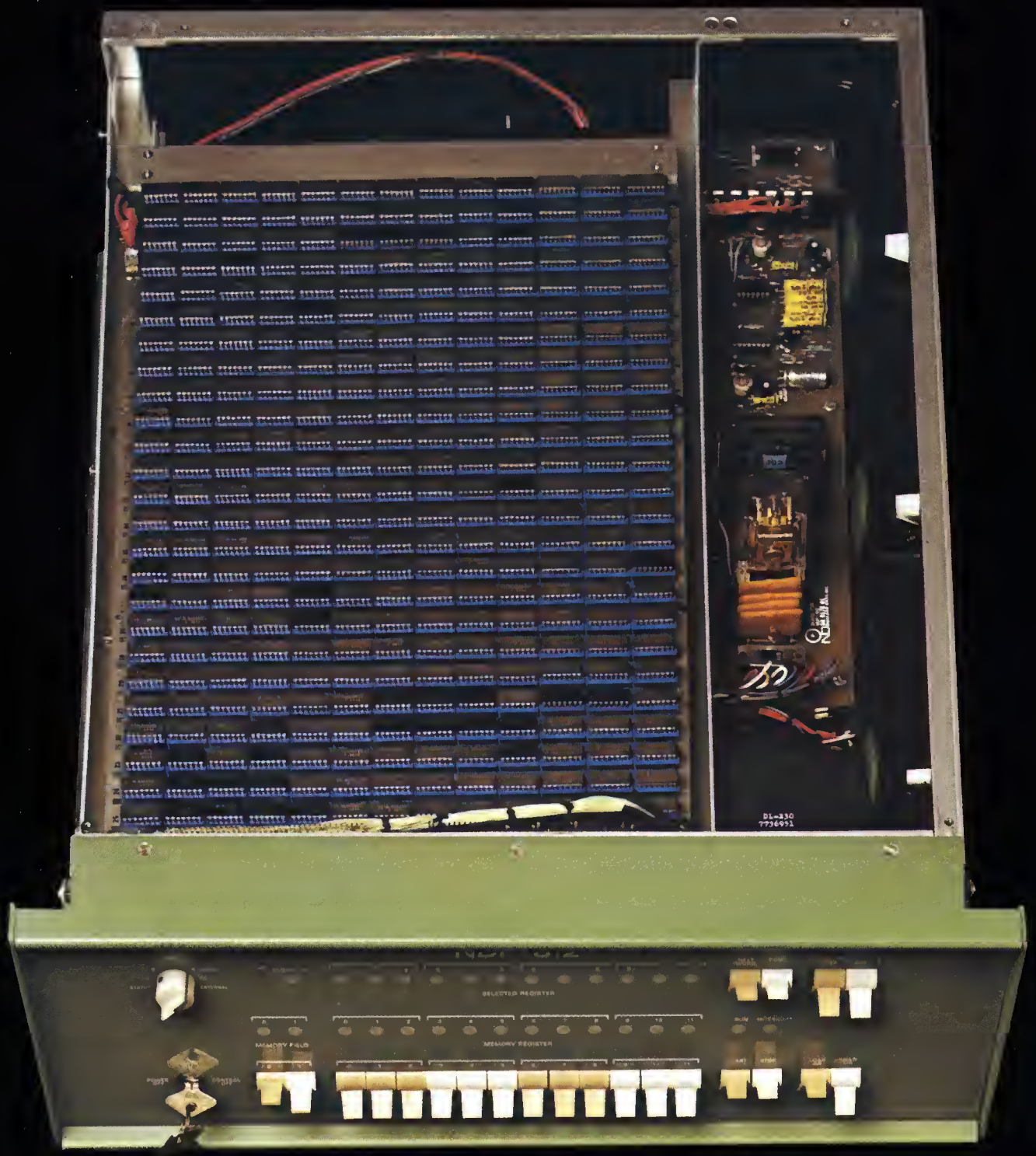
Literal Instructions:

ANDL	21xx	Logical AND last six bits of instruction (xx) with lower six bits of lower accumulator (J), also sets upper six bits of accumulator (J) to zero.
ADDL	22xx	Add last six bits of instruction (xx) to lower accumulator (J).
SUBL	23xx	Subtract last six bits of instruction (xx) from lower accumulator (J).

Numerical and Register Control Instructions:

AJK J	1120	Add upper (K) and lower (J) accumulators and deposit result in lower accumulator (J).
AJK K	1220	Add upper (K) and lower (J) accumulators and deposit result in upper accumulator (K).
AJK JK	1320	Add upper (K) and lower (J) accumulators and deposit result in both accumulators (J, K).
NAJK J	1130	Add upper (K) and lower (J) accumulators, complement and increment the result, and deposit this negation in lower accumulator (J).
NAJK K	1230	Add upper (K) and lower (J) accumulators, complement and increment the result, and deposit this negation in upper accumulator (K).
NAJK JK	1330	Add upper (K) and lower (J) accumulators, complement and increment the result, and deposit this negation in both accumulators (J, K).
SJK J	1121	Subtract upper (K) from lower (J) accumulator and deposit result in lower accumulator (J).
SJK K	1221	Subtract upper (K) from lower (J) accumulator and deposit result in upper accumulator (K).
NSJK J	1131	Subtract lower (J) from upper (K) accumulator and deposit result in lower accumulator (J).
NSJK K	1231	Subtract lower (J) from upper (K) accumulator and deposit result in upper accumulator (K).
ADR J	1122	Add lower sub-accumulator (R) to lower accumulator (J) and deposit result in lower accumulator (J).
ADR K	1222	Add lower sub-accumulator (R) to upper accumulator (K) and deposit result in upper accumulator (K).
NADR J	1132	Add lower sub-accumulator (R) to lower accumulator (J), complement and increment result, and deposit this negation in lower accumulator (J).
NADR K	1232	Add lower sub-accumulator (R) to upper accumulator (K), complement and increment result, and deposit this negation in upper accumulator (K).
ADS J	1124	Add upper sub-accumulator (S) to lower accumulator (J) and deposit result in lower accumulator (J).
ADS K	1224	Add upper sub-accumulator (S) to upper accumulator (K) and deposit result in upper accumulator (K).
NADS J	1134	Add upper sub-accumulator (S) to lower accumulator (J), complement and increment result, and deposit this negation in lower accumulator (J).
NADS K	1234	Add upper sub-accumulator (S) to upper accumulator (K), complement and increment result, and deposit this negation in upper accumulator (K).
SBR J	1123	Subtract lower accumulator (J) from lower sub-accumulator (R) and transfer result to lower accumulator (J).
SBR K	1223	Subtract upper accumulator (K) from lower sub-accumulator (R) and deposit result in upper accumulator (K).
NSBR J	1133	Subtract lower sub-accumulator (R) from lower accumulator (J) and deposit result in lower accumulator (J).
NSBR K	1233	Subtract lower sub-accumulator (R) from upper accumulator (K) and deposit result in upper accumulator (K).
SBS J	1125	Subtract lower accumulator (J) from upper sub-accumulator (S) and deposit result in lower accumulator (J).

View of the ND812 showing front panel, socket board, and power supply. All signals are available at the IC pins and the socket board has no discrete components



Numerical and Register Control Instructions:

SBS K	1225	Subtract upper accumulator (K) from upper sub-accumulator (S) and deposit result in upper accumulator (K).
NSBS J	1135	Subtract upper sub-accumulator (S) from lower accumulator (J) and deposit result in lower accumulator (J)
NSBS K	1235	Subtract upper sub-accumulator (S) from upper accumulator (K) and deposit result in upper accumulator (K)
LJSW	1010	Load lower accumulator (J) from switch register
LJST	1011	Load lower accumulator (J) from status bus
RTST	1002	Restore status bus. Sets flag equal to bit 10 and overflow equal to bit 11 of lower accumulator (J)
LJFR	1102	Load lower accumulator (J) from lower sub-accumulator (R)
LKFJ	1204	Load upper accumulator (K) from lower accumulator (J)
LKFS	1202	Load upper accumulator (K) from upper sub-accumulator (S)
LRFJ	1101	Load lower sub-accumulator (R) from lower accumulator (J)
LSFK	1201	Load upper sub-accumulator (S) from upper accumulator (K)
LJKFRS	1302	Load lower and upper accumulators (J, K) from lower and upper sub-accumulators (R, S)
LRSFJK	1301	Load lower and upper accumulators (R, S) from lower and upper accumulators (J, K)
EXKS	1203	Exchange upper accumulator (K) with upper sub-accumulator (S)
EXJR	1103	Exchange lower accumulator (J) with lower sub-accumulator (R)
EXJRKS	1303	Exchange lower accumulator (J) with lower sub-accumulator (R) and upper accumulator (K) with upper sub-accumulator (S)
Note:		Register control instructions do not require clearing registers to which data is to be transferred, and after transfer the data is left in the source register.
CLR	1410	Set flag to zero
CLR J	1510	Set lower accumulator (J) to zero
CLR K	1610	Set upper accumulator (K) to zero
CLR O	1450	Set overflow bit to zero
CMP	1420	Complement flag
CMP J	1520	Complement lower accumulator (J)
CMP K	1620	Complement upper accumulator (K)
INC J	1504	Increment lower accumulator (J)
INC K	1604	Increment upper accumulator (K)
Note:		The above clear, complement, and increment instructions can be micro-programmed to give a large number of combination instructions of the type shown in the following examples.
CLR CMP J	1530	Clear and complement lower accumulator (J)
CMP INC J	1524	Complement and increment lower accumulator (J) (negation)
CLR JK O	1750	Clear lower accumulator (J), upper accumulator (K) and overflow bit

AND J	1100	Logical AND upper (K) and lower (J) accumulators and deposit result in lower accumulator (J)
AND K	1200	Logical AND upper (K) and lower (J) accumulators and deposit result in upper accumulator (K)
AND JK	1300	Logical AND upper (K) and lower (J) accumulators and deposit result in both accumulators (J, K)
MPY	1000	Hardware multiply: 12 bit multiplier in lower accumulator (J) 12 bit multiplicand in upper accumulator (K) 24 bit product in sub-accumulators (R, S)
DIV	1001	Hardware divide: 12 bit divisor in lower sub-accumulator (R) 23 bit dividend in accumulators (J, K) 12 bit quotient in lower accumulator (J) 12 bit remainder in upper accumulator (K)

Shift and Rotate Instructions:

SFTZ J	1140	Shift zeroes left into lower accumulator (J). (Number of zeroes shifted determined by coded last four bits of instruction, giving a choice of 0 to 15 bits shift.)
SFTZ K	1260	Shift zeroes left into upper accumulator (K). (As above, a choice of 0 to 15 bits shift.)
SFTZ JK	1340	Shift zeroes left into lower accumulator (J). (As above, choice of 0 to 15 bits shift.) Lower accumulator (J) shifts into upper accumulator (K).
ROTD J	1160	Rotate data in lower accumulator (J). (As above, number of bits rotated determined by last four bits of instruction, giving a choice of 0 to 15 bits rotation.)
ROTD K	1260	Rotate data in upper accumulator (K). (As above, choice of 0 to 15 bits rotation.)
ROTD JK	1360	Rotate data in both accumulators (J, K) as a 24-bit register. (As above, choice of 0 to 15 bits rotation.)

Control Instructions:

IDLE	1400	One-cycle delay.
PION	1500	Power interrupt ON
PIOF	1600	Power interrupt OFF
STOP	0000	Stop

Skip Instructions:

SIZ	1405	Skip if flag is zero
SIZ J	1505	Skip if lower accumulator (J) is zero
SIZ K	1605	Skip is upper accumulator (K) is zero
SIZ O	1445	Skip if overflow bit is zero
SNZ	1401	Skip if flag is not zero
SNZ J	1501	Skip if lower accumulator (J) is not zero
SNZ K	1601	Skip if upper accumulator (K) is not zero
SNZ O	1441	Skip if overflow bit is not zero
SIP J	1502	Skip if lower accumulator (J) is positive or zero (most significant bit is zero)
SIP K	1602	Skip if upper accumulator (K) is positive or zero (most significant bit is zero)

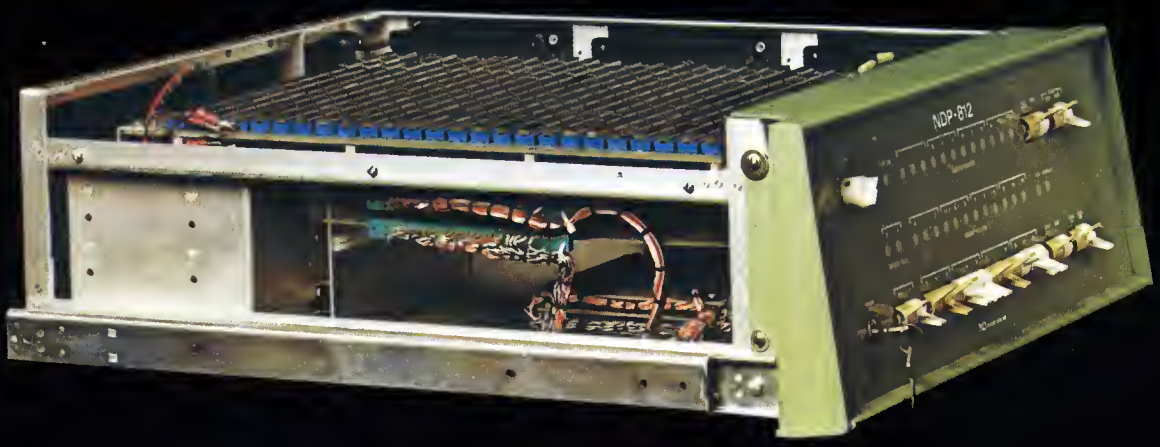
1. Side view of the ND812 showing memory compartment with 4K stack. An 8K memory would occupy the same compartment. Memory systems are field expandable

2. Open rear view of the ND812. On the right is an I/O bin with connectors capable of holding three 7" x 5" printed circuit boards for peripheral or customer interfaces

3. Front view of the ND812 showing plastic front panel removed for easy access to front panel board components For system compatibility users may replace this plastic front panel with one of their own color and design

4. Front view of the ND812 showing the front panel board disconnected for dedicated OEM applications. The processor can be remotely controlled via the I/O connector

1.



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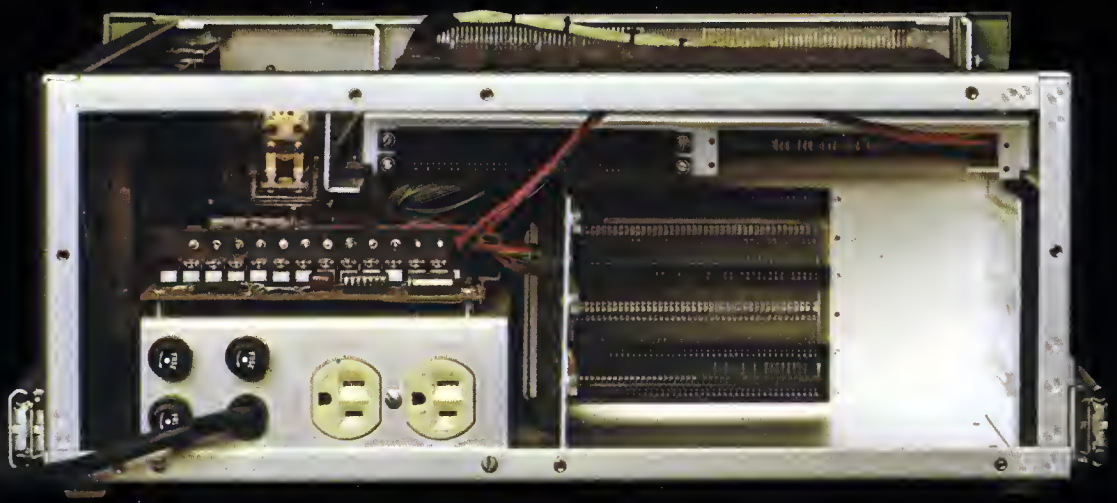

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1. Side view of the ND812 showing memory compartment with 4K stack. An 8K memory would occupy the same compartment. Memory systems are field expandable

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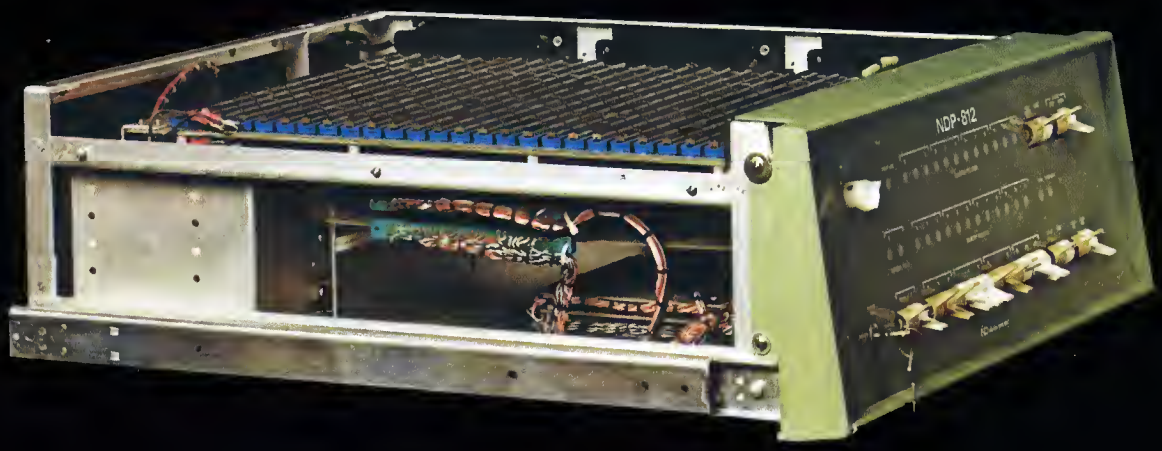

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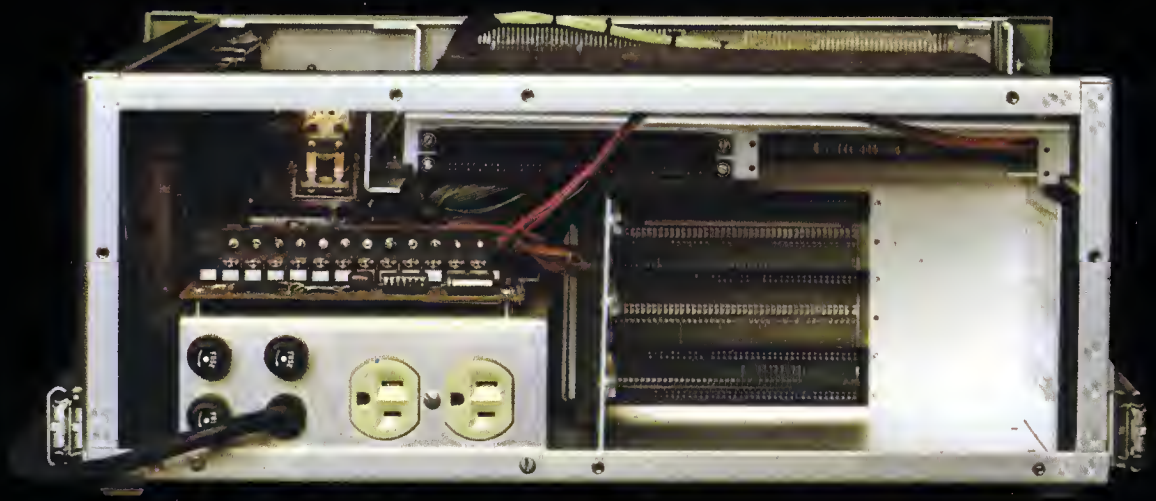


Skip Instructions:

SIN J	1506	Skip if lower accumulator (J) is negative (most significant bit is one)
SIN K	1606	Skip if upper accumulator (K) is negative (most significant bit is one)
SKPL	1440	Skip on Power Low
SIP O	1442	Unconditional skip

Note: These skip instructions can be micropragrammed to give a large number of combination instructions of the type shown in the following examples.

SIN SIZ J	1507	Skip if lower accumulator (J) is negative or zero
SIP SNZ J	1503	Skip if lower accumulator (J) is positive and not zero

Priority Interrupt Instructions:

IOFF	1003	Turn Interrupt OFF
IONN	1004	Highest level interrupt enabled
IONA	1006	Highest level and special level A interrupts enabled
IONB	1005	Highest level and special level B interrupts enabled
IONL	1007	Highest level, special level A, special level B, and lowest level interrupt enabled

I/O Instructions: The last four bits of each I/O instruction may be used to provide voltage levels for device selection and they may also be used to generate four sequential pulses for peripheral control. These pulses make multi-function operation possible with a single I/O instruction. A typical example for a single instruction would be SKIP, READ, and CLEAR FLAG.

The Peripheral Control Pulses (PCP's) are used as follows:

PCPO: May be used for skip or control of peripheral devices

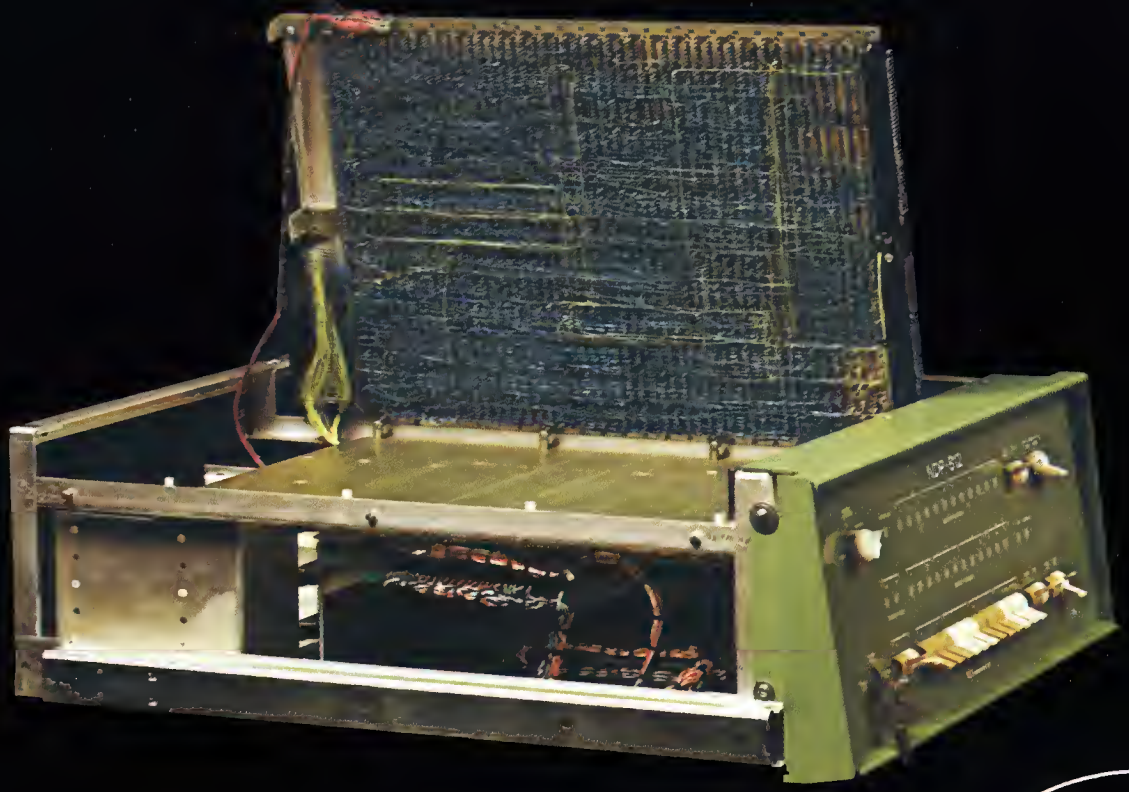
PCP1 and PCP2: May be used for any I/O function. Generally used for skip conditions and data transfer.

PCP3: To be used for internal peripheral control.

Note: When the last four bits of an I/O instruction are used to provide voltage levels for device selection, a total of 256 I/O commands at 3 μsec per instruction are possible using single word instructions, and a total of 4096 commands at 5 μsec per instruction are possible using two-word instructions.

ND812 SPECIFICATIONS

Type:	Digital stored-program general-purpose computer.
Memory:	Magnetic core, 8192 words, 12 bits, 2 μsec cycle time. *Memory options:* Minimum 4K, expandable in the field to 16K in 4K increments.
Price:	The price of less than $10,000 includes complete processor with 8K memory, teletype interface, and software as listed below. Hardware multiply and divide and 4-level priority interrupt are standard features.
Addressing:	Relative, indirect, and direct. Hardware multiple field control.
Arithmetic:	Parallel, binary, fixed point, 2's complement. Hardware multiply and divide are standard features.
Instructions:	Single and double word instructions which include sixteen memory reference instructions, three literals, and more than fifty arithmetic and register control instruction. The instruction set is shown on pages 3 through 10.
Input/Output:	Interrupt: Programmable 4-level priority interrupt. Trap to any core location in first 4K of memory. Programmed I/O transfer: Capability per single I/O instruction: Transmit 12 or 24 bits Receive 12 or 24 bits Transmit 12 *and* receive 12 bits Receive 12 *and* transmit 12 bits I/O instruction includes four (4) microprogrammable pulses for multi-function operation with a single instruction. With single-word instructions there are 256 possible I/O commands at 3 μsec per instruction. With two-word instructions there are 4096 possible I/O commands at 5 μsec per instruction. Total of 75 control, data, and sense lines available on a single connector. Direct Memory Access (DMA): 6 megabits per second; Read, load, increment or *decrement* on DMA on a single cycle.
Accumulators:	Dual accumulators with individual sub-accumulators.
Control Panel:	Constant display of memory register with switch-selected display of six other registers and two busses. Front panel removable key lock. Power off, on, panel lock. Removable front panel for dedicated O.E.M. applications.
Timing:	16 MHz crystal controlled clock insures absolute timing and drift-free operation.
Software:	Includes Assembler, Editor, utilities, diagnostics, Integer Arithmetic Package, Floating-Point Package, and NUTRAN interpretative compiler
Servicing:	Central processing unit uses 97% MSI and TTL integrated circuitry with no discrete components. Entire CPU complement of IC's is mounted on a single wire wrapped *socket board,* thus making every signal available and permitting simple replacement of IC's without soldering.
Reliability:	The ND812 provides a new level of reliability by means of an accelerated-life test technique. Before shipment every integrated circuit is subjected to power operation at elevated temperatures equivalent to six months normal continuous operation. What would have been early failures in the field are thus discovered before shipment, resulting in greatly increased reliability.
Expansion:	Main frame capable of 4K or 8K operation. Expansion beyond 8K uses an additional identical enclosure.
Miscellaneous:	Program controlled hardware flag (single bit register). Programmable power-failure interrupt. Two auto-increment locations for each 4K of core.



1

3

2

Dimensions:	Processor, including memory and power supply: 19″ wide x 7″ high x 22″ deep. Standard unit has slides for rack mounting in standard 19″ wide rack.
Weight:	60 lbs.
Power Consumption:	400 watts @ 115/230V 50/60 Hz
Environment:	Operating temperature range 10°C to 50°C
Note:	All features listed in the above specifications are standard in the ND812
Peripherals:	Peripherals for which interfaces are available: Teletype IBM Selectric I/O Writer High Speed Punch High Speed Reader Disc Computer Compatible Magnetic Tape Digital Cassette Recorder Analog-to-Digital Converters Digital-to-Analog Converters Graphic Display Light Pen Line Printer Analog Plotter For users who wish to add their own peripherals and interfaces, an I/O bin is available to accommodate enough printed circuit modules for several interfaces.
The following options are also available:	
Options:	Memory Expansion Hardware Program Loader (requires no core) Power Restart Hardware ODA (Octal Debugging Aid) Real Time Clock Cassette and Disc operating systems Special applications software packages

1. View showing underside of the ND812 socket board. Wiring is done by semi-automatic wire-wrap machine, giving low cost error-free wiring

2. View of the ND812 showing socket board raised. The central Processing Unit uses 97% MSI and TTL and 3% DTL integrated circuitry

3. Replacing an IC in the ND812 socket board. No unsoldering or resoldering required. No printed circuit boards or modules necessary as spare parts

ND812 WORD FORMATS

Single-Word Memory Reference Instructions

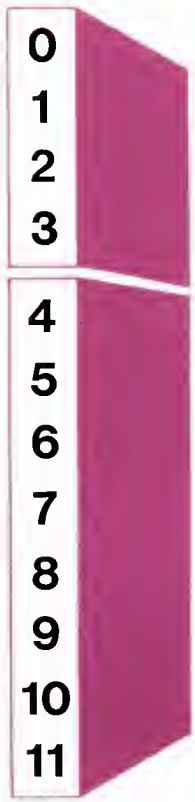
Instruction code

Direct or indirect addressing

Forward or backward (see 'relative address' below for explanation)

Relative address. These six bits are added to or subtracted from (depending on the state of bit 5) the contents of the Address Register to give the effective operand address

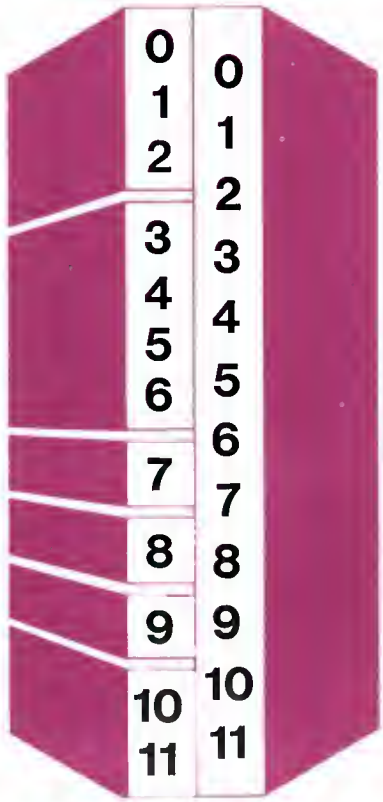
Single-Word Operating Instructions



Instruction code

These eight bits are combined to provide various register control instructions such as SHIFT or ROTATE, with choice of from 0 to 15 bits shift or rotate, SKIP, logical AND, logical OR, LOAD, EXCHANGE, ADD, SUBTRACT, SET, CLEAR, COMPLEMENT, INCREMENT, and 12 or 24-bit accumulator operation

Two-Word Memory Reference Instructions



Operation code

Instruction code

Direct or indirect address

Upper accumulator

Field change

Field selection

Absolute address

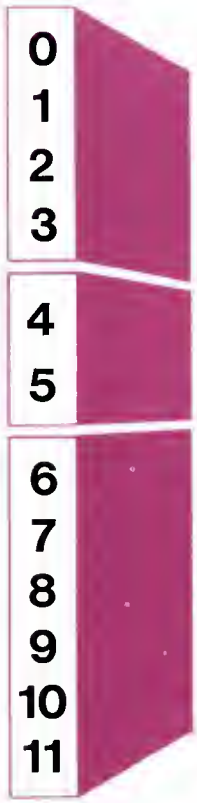
Single-Word I/O Instructions

Instruction code

Device selection code

These four bits may be used to provide voltage levels for device selection codes. In combination with bits 4-7 above they provide a total of 8 bits or 256 I/O commands
These four bits may also be used to generate four sequential pulses for peripheral control, giving multi-function operation with a single I/O instruction

Single-Word Literal Instructions



Operation code

Instruction code

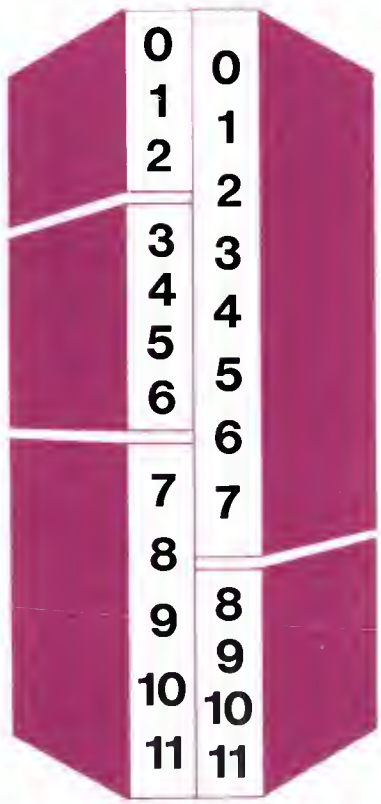
These six bits represent the actual operand, not the address of the operand

Two-Word I/O Instructions

Operation code

Instruction code

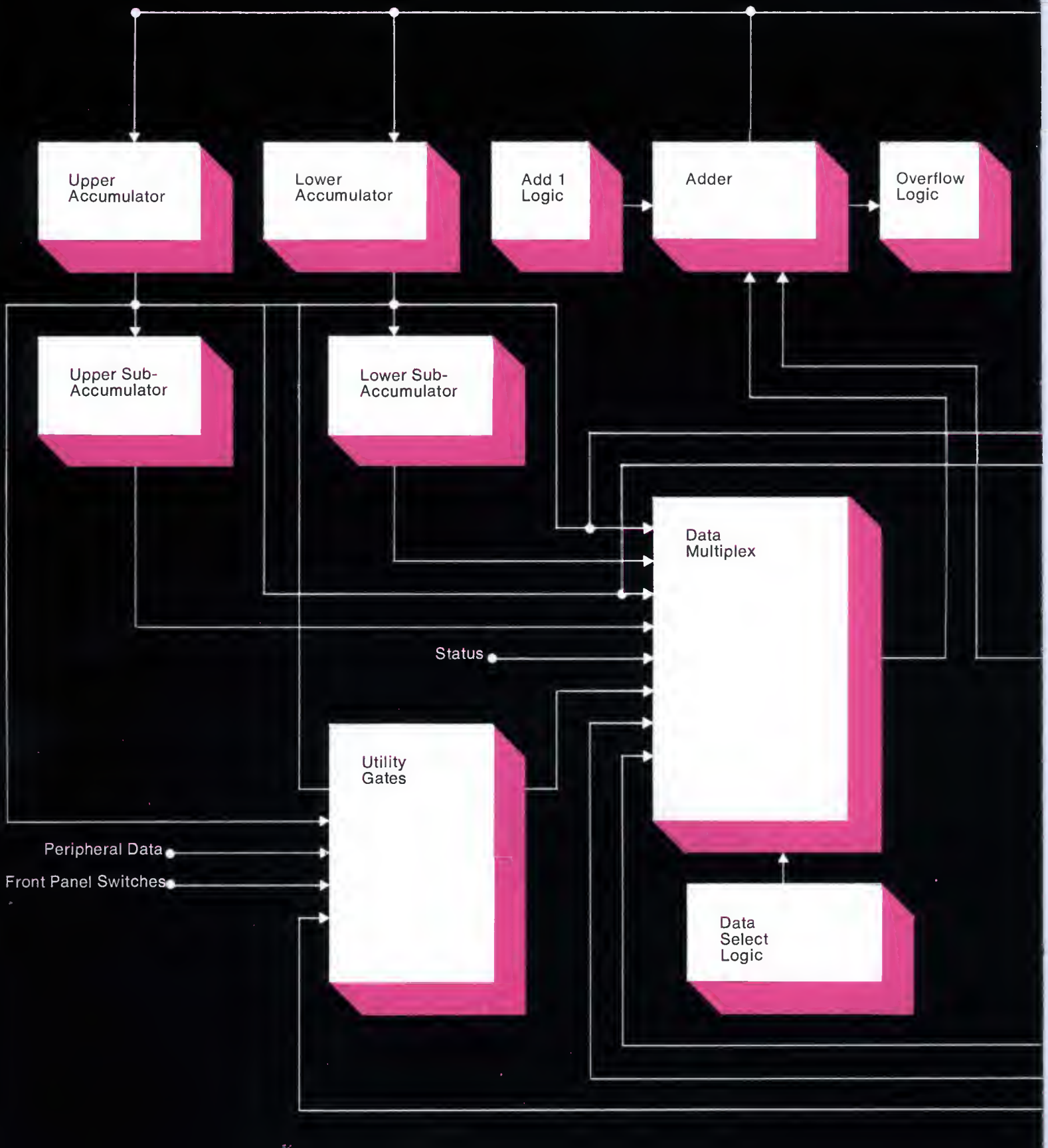
Unused

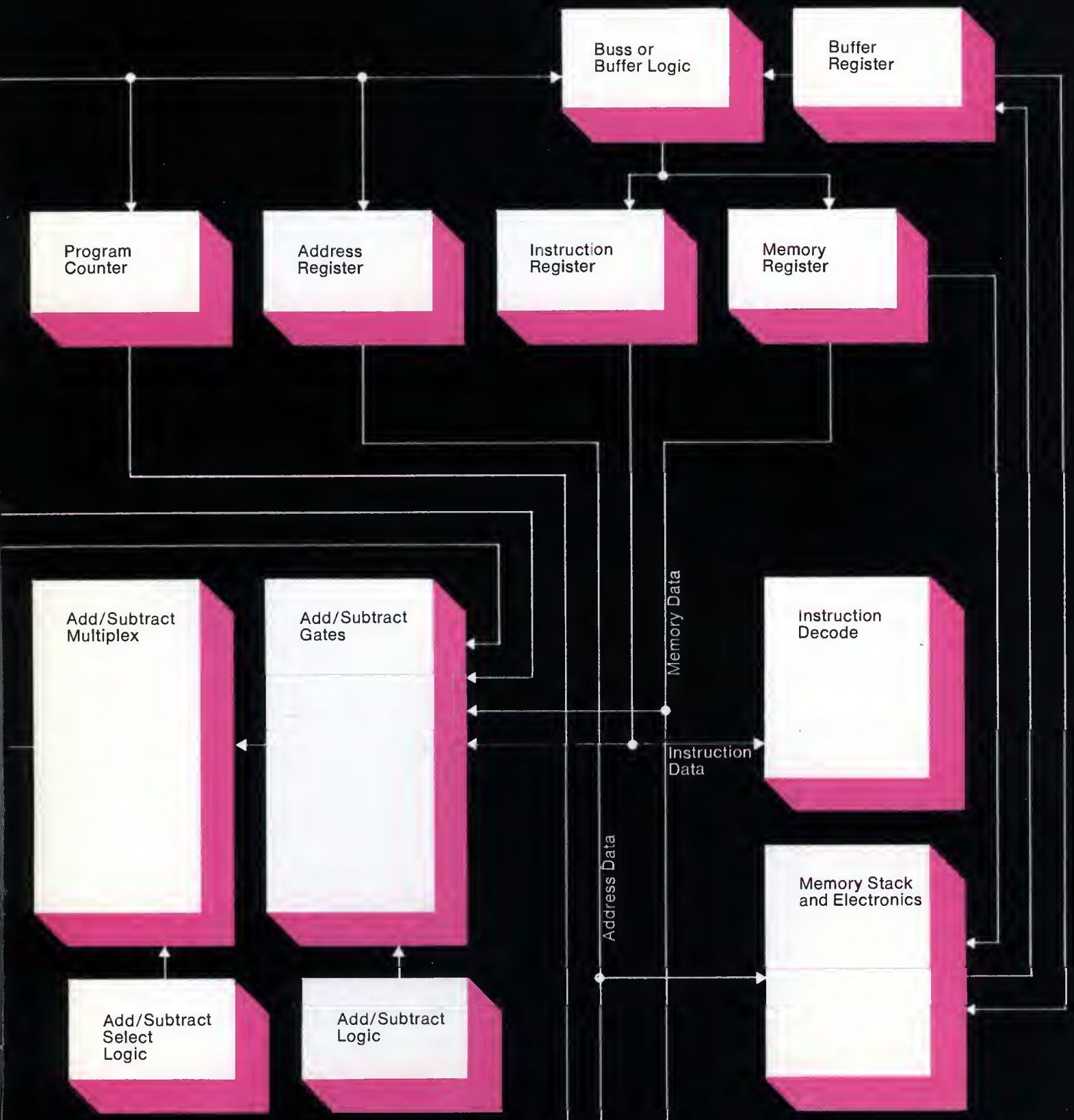


Device selection code
8 bits gives 256 I/O commands

These four bits may be used for device selection. In combination with bits 0-7 they give 4096 I/O commands.
These four bits may also be used to generate four sequential pulses for peripheral control, providing multi-function operation with a single I/O instruction.

ND812 BLOCK DIAGRAM




Buss or Buffer Logic
Buffer Register
Program Counter
Address Register
Instruction Register
Memory Register
Add/Subtract Multiplex
Add/Subtract Gates
Memory Data
Instruction Decode
Instruction Data
Address Data
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